METHODS OF TESTING FOR SHORTS IN PROGRAMMABLE LOGIC DEVICES USING RELATIVE QUIESCENT CURRENT MEASUREMENTS

ABSTRACT

Methods of testing for shorts (e.g., bridging defects) between interconnect lines in an integrated circuit. For example, in a design implemented in a programmable logic device (PLD), some interconnect lines are used and others are unused. To test for shorts between the used and unused interconnect lines, both used and unused interconnect lines are driven to a first logic level, and the leakage current is measured. The used interconnect lines are driven to a second logic level, while the unused lines remain at the first logic level. The current is again measured, and the difference between the two measurements is determined. If the difference exceeds a predetermined threshold, the device/design combination is rejected. Some embodiments provide methods of testing for shorts between used and unused interconnect lines for a design targeted to a partially defective PLD.